System Comparison of Electronic and Optical Correlator

Yun-Parn Thomas Lee

Journal of Signal Processing Systems
for Signal, Image, and Video Technology
(formerly the Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology)

ISSN 1939-8018
Volume 66
Number 2

J Sign Process Syst (2012) 66:93-98
DOI 10.1007/s11265-010-0571-9

Springer

J Sign Process Syst (2012) 66:93–98
DOI 10.1007/s11265-010-0571-9

System Comparison of Electronic and Optical Correlator

Yun-Parn Thomas Lee

Received: 22 August 2009 / Revised: 12 October 2010 / Accepted: 9 December 2010 / Published online: 24 December 2010

Abstract During the past three decades, optical information processing has received a lot of attention from large number of engineers and physicists. Although both optical coherent and incoherent processing can be employed for optical correlation and convolution, and wide variety of information processing functions can be performed, however, several new faster approaches to VLSI implementation of electronic cross correlation or convolution have been demonstrated recently. Due to increasingly importance of correlator in apply to digital image processing, stereo matching, and pattern recognition. In this paper, we perform a comparison between the electronic and optical correlator in terms of several system parameters, such as timing, area and power consumption. Such comparison may assist the system planner in actual implementation

Keywords Optical correlator · Two dimensional electronic correlator · VLSI

1 Introduction

The cross correlation or convolution function play extremely important role in the modern technology of digital image processing and computer vision. In preprocessing of image data, image features at different levels of complexity are extracted from the image data, typical examples of such features are lines, edges and ridges. The line features can be readily available by cross convolution of a LOG (Laplace of Gaussian) with gray level image.

In the area of image detection and segmentation, convolution function also play an important role, selection of a specific set of interest point or segmentation of multiple image regions which contain a specific object of interest, we only need to use certain filter functions to convolve with the desired images.

The cross correlation (or convolution) between the input image and the filter function can be written in continuous format as shown in the following equations,

$$f(x,y) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} k(x+\xi, y+\eta) i(\xi,\eta) d\xi d\eta \tag{1}$$

$$f(x,y) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} k(x-\xi, y-\eta) i(\xi,\eta) d\xi d\eta \tag{2}$$

Equation 1 stands for the cross correlation, Eq. 2 stands for the cross convolution. Or, in the discrete format, we may rewrite above continuous format as shown below:

$$f_{mn}^{pq} = \sum_{\xi=1}^{A}\sum_{\eta=1}^{B} k_{mn}^{pq\xi\eta} i_{\xi\eta} \tag{3}$$

In Eq. 3, we are using high dimensional generalized tensor inner product notation. The indices ξ=1,2,...A, η=1,2,...B are local indices of each pixel of input images, the two indices p and q are used to index the submatrix of the correlation filter. The cross correlation calculation is equal to the multiple stages of the multiply and add operation, and this operation can write the equivalent mathematical notation as $f \leftarrow f + k \times i$.

Y.-P. T. Lee (✉)
Department of Electronic Engineering, Ming Chuan University, Taoyuan, Taiwan 333, Republic of China
e-mail: yplee@mail.mcu.edu.tw

2 Advantages and Disadvantages of Using Optical Correlator

In a 4f coherent optical correlator [1–4], there are two fundamental techniques, the first one uses the holographic match filtering, and the second one uses the joint transform correlator. In Fig. 1, the input plane consists of programmable magneto optic spatial light modulator (MOSLM), MOSLM is a passive optical device. This device modulates the light source of laser according to the input electrical signal. The distance between MOSLM and the first Fourier transform lens is f_1, this is the same distance between Fourier transform lens and liquid crystal light valve (LCLV). Also, the distance between LCLV and the output CCD detector plan is f_2. The fourier transform and the inverse of fourier transform are taking place in between the MOSLM and CCD detector plane, thus forms the operation of cross convolution.

Typical 4f coherent optical correlator is bulky and difficult to use. This disadvantage can be improved by using the geometrical shadow casting optical convolver [5].

Please refer to Fig. 2, the geometrical shadow casing convolver using a single lens instead of using two lens in optical correlator. Since the plane of convolution can occur anywhere between the focal point of the lens and the convolution kernel, through a simple calculation, we can easily calculate the area of the output plane of the convolver. Let us assume the diameter of the lens is D, the focal length of the lens is f, the distance between input plane and the convolutional kernel spatial light modulator is d_1, also, the distance between the convolutional kernel spatial light modulator and the detector array is d_2. The length of the convolution plane on the detector array can be calculated as

$$\frac{\frac{x}{2}}{f-d_2}=\tan\theta=\frac{\frac{D}{2}}{f}\ or\ x=D\frac{(f-d_2)}{f} \tag{4}$$

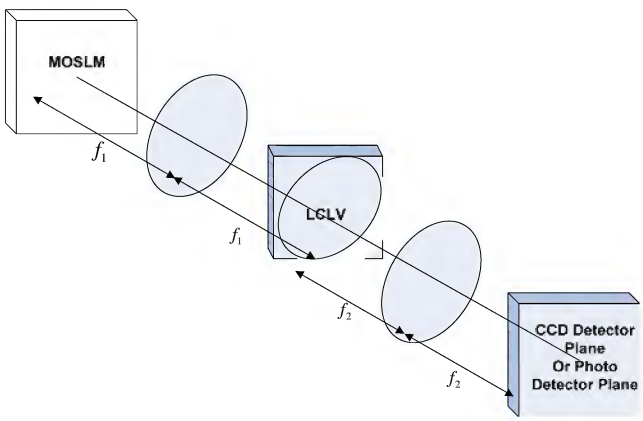

Figure 1 A 4f coherent optical correlator.

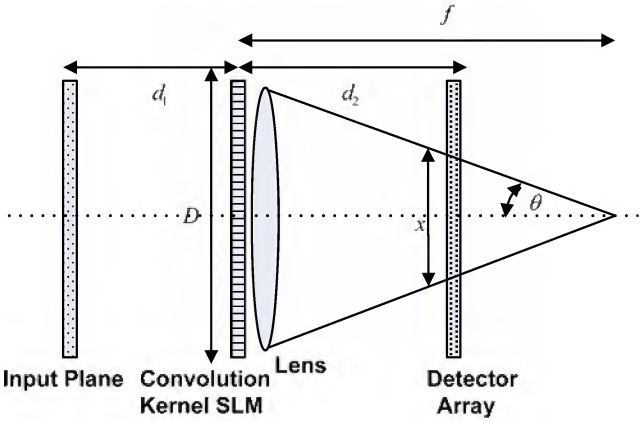

Figure 2 The geometrical shadow casting convolver.

So the computational area must bounded to be $D^2\frac{(f-d_2)^2}{f^2}$. The computational area is mainly limited by three components of the system parameters: focal length f, the diameter of lens D, and the distance between the convolutional kernel and the detector array d_2. Assume the area of the smart modulator and driver is A_{mod}, the detector area is A_{det}, and the amplifier area is A_{amp}, then the following lower bound relation must hold :

$$A_{\mathrm{mod}}+A_{\mathrm{det}}+A_{amp}\le D^2\frac{(f-d_2)^2}{f^2} \tag{5}$$

The computational volume is bounded to $D^2(d_1+d_2)$on the geometrical shadow casting optical convolver. Therefore, the computational volume can be estimated as

$$V=3D^2(d_1+d_2) \tag{6}$$

For an optoelectronic system with the source and the detector, the total power consumption of the optoelectronic system can be calculated as following:

$$P_{OE}=P_{\mathrm{mod}}+P_{\mathrm{det}}+P_{amp} \tag{7}$$

$$P_{\mathrm{mod}}=K_LC_mV_m^2F=\Phi_{\mathrm{mod}}(N,A_{\mathrm{mod}}) \tag{8}$$

$$P_{\mathrm{det}}=I_{\mathrm{det}}V=\varphi_{\mathrm{det}}(N,A_{\mathrm{det}}) \tag{9}$$

Since $P_{\mathrm{mod}}+P_{\mathrm{det}}\gg P_{amp}$, therefore, we have

$$P_{OE}=P_{\mathrm{mod}}+P_{\mathrm{det}} \tag{10}$$

Where in Eq. 7 to 10, P_{mod} represents the power consumption of the modulators, P_{det} represents the power consumption of the detector, P_{amp} represents the power consumption of the processing circuits, C_m represents the modulator capacitances, F stands for the system clock speed, V_m is the modulator operating voltage, and K_L is the

modulator operating coefficient. Equation 7 indicates that the total power consumption is equal to the summation of the power of modulator, the power of detectors and the power of electronic amplifier. Equation 8 states that the power of modulator is a function of capacitance, modulation voltage and modulation frequency of spatial light modulator. Equation 9 indicates the power consumption of detectors is a function of number of pixels and area of detectors.

The latency of the optoelectronic system can be represented as following:

$$t_{OE} = t_{\mathrm{mod}} + t_{\mathrm{det}} + t_{amp} \tag{11}$$

In above equation, t_{mod} represents the response time of the modulators, t_{det} represents the time delay of the detector, and t_{amp} represents the response delay of the processing circuits.

Since the data presenting to the input and output planes of optoelectronic system are mostly analog gray level or binary, so the computational accuracy of the optoelectronic system is indeed a serious problem to be solved. There are new methods proposed to solve this problem, however, the computational accuracy needs further enhancement in order to be competed with VLSI electronic correlator.

3 Advantages and Disadvantages of Using Electronic Correlator

In electronics, many researchers worked on 2-D convolver chips, there are two major methods to perform cross correlation or convolution, the first one uses a cascaded mechanism of the Fourier transform and inverse Fourier transform [6], which include a transformation unit and a cross correlator controller, due to the inherent nature of the Fourier transform, the data are further divide into the real part and the imaginary part, This method is rather complicated and time consuming.

Second method is using multiplierless 2-D convolver, Myung H. Sunwoo [7] proposed using shifter and accumulator to replace the multiplier, although their convolver can outperform HSP48901 and HSP48908, however, Samsung's chip has limitation on kernel size.

Zhang proposed a new method [8–11]. The electronic convolver performs logarithmic computations by utilizing novel log and inverse-log modules, therefore to eliminate the hardware multiplier in the system. This new approach can reduce VLSI area and power significantly, while maintaining the kernel size. The new architecture with pipelined design can produce output in every clock cycle. However, Zhang's work did not fully analysis the performance of his electronic convolver, nor did he compare with the optical correlator. Therefore, I present the analysis in this section.

According to mathematical definition, the logarithm of x to the base b is shown as $\log_b x$; an important nature of logarithms can change complicated multiplication to addition operation

$$\begin{aligned} &\log_b xy = \log_b x + \log_b y \ \mathrm{Or} \\ &x^* y = \log_b{}^{-1}[\log_b x + \log_b y] \end{aligned} \tag{12}$$

Therefore the complicated 2-D convolution can reduce to the following equation, assume logarithm's base is 2, then Eqs. 1 and 2 in the first section becomes

$$F(m,n) = \sum_{i=-(M-1)/2}^{(M-1)/2} \sum_{j=-(N-1)/2}^{(N-1)/2} K(i,j) I(m-i, n-j) \tag{13}$$

Or,

$$F(m,n) = \sum_{i=-(M-1)/2}^{(M-1)/2} \sum_{j=-(N-1)/2}^{(N-1)/2} 2^{\log_2[K(i,j)] + \log_2[I(m-i,n-j)]} \tag{14}$$

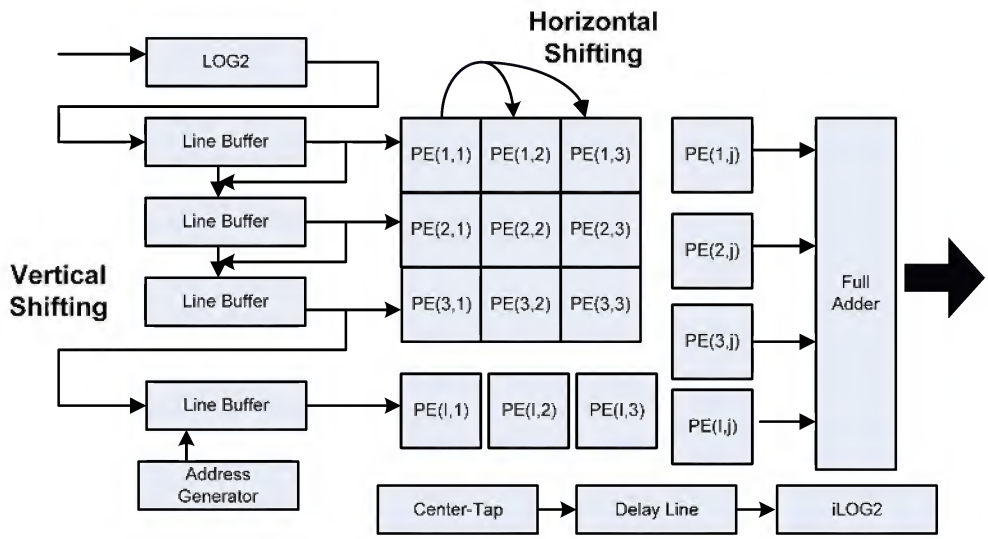

Figure 3 2-D VLSI Electronic Correlator Architecture.

Table 1 Comparison table of 2-D multiplierless electronic correlator.

System comparison	Optoelectronic correlator	2-D multiplierless electronic correlator
Convolver		
Power	$P_{OE} = P_{\mathrm{mod}} + P_{\mathrm{det}}$ Where $P_{\mathrm{det}} = I_{\mathrm{det}} V = \varphi_{\mathrm{det}}(N, A_{\mathrm{det}})$	$P_{2D\_Convolver} = MP_{LB} + MNP_{PE} + P_{LOG} + P_{LOG}{}^{-1} + P_{adder}$
Area	$A_{\mathrm{mod}} + A_{\mathrm{det}} + A_{amp} \leq D^{2\frac{(f-d_2)^2}{f^2}}$	$A_{2D\_Convolver} = MA_{LB} + MNA_{PE} + A_{LOG} + A_{LOG}{}^{-1} + A_{adder}$
Speed	$t_{OE} = t_{\mathrm{mod}} + t_{\mathrm{det}} + t_{amp}$	$t_{2D\_Convolver} = t_{LB} + Mt_{PE} + t_{LOG} + t_{LOG}{}^{-1} + t_{adder}$
Accuracy	Can only work in fixed point integer or binary	Floating Point
Advantages	Speed is fast, only limited by Spatial light modulator and detector	Accurate, speed may achieve frame rate
Disadvantages	Bulky	Larger Power Consumption

So, the $\log_2$ and inverse $\log_2$ modules are very important components in the two dimensional multiplier-less correlator design. In Fig. 3, we demonstrate the architecture of a multiplier-less two dimensional cross correlator, please note this correlator can compute the floating point calculation in real time. The data come into the system first by going through $\log_2$ module, then the output data stream pass through the line buffers. These line buffers are managed by an address generator, the outputs of line buffers are simultaneously fed into arrarys of processing element. The outputs of these processing element arrarys are summed by a pipelined adder, which can increase the speed dramatically.

Assume M stands for the number of rows of processing elements, N stands for the number of columns of processing elements. The VLSI area of line buffer is A_{LB}, the area of each processing element is A_{PE}, the area of Log module is A_{LOG}, the area of inverse Log module is $A_{LOG}{}^{-1}$, and the area of the pipelined adder is A_{adder}, then the total area of this 2-D multiplierless convolver is

$$A_{2D\_Convolver} = MA_{LB} + MNA_{PE} + A_{LOG} + A_{LOG}{}^{-1} + A_{adder} \quad (15)$$

Also, the power consumption of this VLSI can be estimated as

$$P_{2D\_Convolver} = MP_{LB} + MNP_{PE} + P_{LOG} + P_{LOG}{}^{-1} + P_{adder} \quad (16)$$

Where in equation, the power of line buffer is P_{LB}, the power of each processing element is P_{PE}, the power consumption of Log module is P_{LOG}, the power consumption of inverse Log module is $P_{LOG}{}^{-1}$, and the power a of the pipelined adder is P_{adder}.

For pipelined processing, the primary source of latency delay is due to Log module, the inverse Log module and the full adder, plus the column of array of

Table 2 System symbols used in calculation.

Nomenclature	
t_s	Response time per source's pixel (VCSEL or modulator)
t_d	Response time per detector
K_L	Modulator proportional coefficient
D	Len's diameter
f	Len's focus length
d_1	The distance between the input plane to convolutional kernel
d_2	The distance between the convolutional kernel and the detector array
F	Optical modulator frequency
C_m	Optical modulator Capacitance
V_m	Applied Voltage to Modulator
P_S	Power consumed per source's pixel
P_{mod}	Power consumed on the optical modulator
P_{amp}	Power consumed on the amplifier of optical modulator
P_D	Power consumed on detectors
A_S	Area occupied per source's pixel
A_D	Area occupied per detector
A_{amp}	Area occupied on the amplifier of optical modulator
A_{LB}	VLSI Area occupied by liner buffers
A_{LOG}	VLSI Area occupied by Log Functions
$A_{LOG^{-1}}$	VLSI Area occupied by Anti Log Functions
A_{PE}	VLSI Area occupied by each processing eleme
A_{adder}	VLSI area occupied by adder
$A_{2D\_Convolver}$	VLSI Area occupied by a 2-D convolver
$t_{2D\_Convolver}$	Total time delay of a 2-D convolver
$P_{electronics}$	Total power consumed by electronics
M	Number of Columns in 2-D convolution
N	Number of Rows in 2-D convolver

processing elements, therefore, the time delay of this VLSI is about

$$t_{2D\_Convolver} = t_{LB} + Mt_{PE} + t_{LOG} + t_{LOG}{}^{-1} + t_{adder} \quad (17)$$

According to Ming Zhang [9], this VLSI can run at clock speed 99 MHz of 16 bits resolution and 99 Mpixels/sec, which is outperform than HSP48901 and HSP48908. In order to understand this new 2D multiplier-less convolver's performance, we take MPEG-2 as an example. In MPEG-2 (CCIR601), system can only run at 720x480 pixels, and 30 frames/second, that is 10.4 Mpixels/sec.

4 System Comparison Between Optical and Electronic Correlator

From above discussion, we derive the equations of power, occupied area, and computational latency of both optoelectronic system and 2-D VLSI electronic multiplier less correlator. We can easily see, optoelectronic system has less accuratcy than electronics correlator. Unless a new breakthrough in VCSEL and spatial light modulator of the optoelectronic system, otherwise, the electronic correlator shows much better arithmetic accuracy while still can maintain the high speed competency. A comparison table is shown in Table 1.Nomenclature used in calculation is shown in Table 2.

5 Conclusion

There were many existing practical examples of electronic correlators [8, 12, 13] and optical correlator or hybrid optical-digital correlator [14, 15] in the listed publications [12–15], however, we are lack of comparison results for design engineers in practical applications of image processing and pattern recognition.

Consider an example of a calculation comparing the optical correlator and electronic correlator. According to Zhang [8–10], the electronic VLSI correlator they constructed base on Xilinx VirtexII FPGA, the system consumes 59% of logic slices, 30% of flip-flop, 34% of look up tables, also, the system is capable of 180.9 million pixels per second (mpps) operation, power consumption is about 30.6 watts at 1.5 volts. With a throughput of 1024× 1024 frames, this is equivalent to 172 frames per second. For an optical correlator, depends on using LCLV or VCSEL or spatial light modulator (SLM) as optical input, and different types of photodetector arrays as optical output, we may have different latency, area, and power consumption. If we use LCLV or SLM, the response time is slow, typically, this is about 100 ms, therefore, total latency is about 100 ms. However, if we using Finisar's VCSEL [16] as the optical source. Their rise time and fall time are 40 ps and 40 ps respectively. The area occupied per source pixel is 0.25 mm^2. We use Alphala's ultrafast photodetector [17] as the detector. We choose 100 ps as response time, and 0.25 mm^2 for single detector's area. Assume we use of 128× 128 for optical inputs and outputs, f=20 cm, D=5 cm, d_2= 5 cm, therefore, with single lens correlation, the area is bound to 14.1. The total area for optical input and output is about 8192 mm^2 plus the electronic component's size. The total latency will be 140 ps plus the electronic component's delay. If we use 2 mW per VCSEL [16], and 1 mW per detector [17], the total consumed power is approximately 49.2 W.

Scaling effect [18–21] has received a lot of attention in VLSI interconnect. Scaling effect concluded that "the average feature size drops by a scaling factor of *1/S*, device performance is enhanced as gate delay reduced by a factor of *1/S*, and power dissipation by a factor of $1/S^2$", therefore, more devices can be packed on a chip. However, from our calculation, optical correlator or hybrid digital optical correlator, unlike the VLSI electronic correlator, scaling effect plays very limited role on overall performance [21]. The system speed of VLSI correlator is more determined by the interconnection length, VLSI architecture and its size. These are shown in Eq. 15 to 17.

This paper compares the performance of optical correlator and electronic correlator in terms of power, area and speed. Due to continue improvement on new arithmetic architecture, we concluded that electronic correlator has smaller area and power than optoelectronic system; the consuming power of VCSEL and photodetectors may be higher than electronic VLSI, while VLSI electronic correlator maintain high speed throughput at video frame rate. The major disadvantage of the optoelectronic system is the computational accuracy.

Therefore, we concluded that in future engineering design work for real time pattern recognition, or a digital image processing applications, electronic VLSI system design does demonstrate many practical preferences over the optoelectronic system.

References

1. Goodman, J. W. (2005). *Introduction to fourier optics*, 3rd edn. Roberts & Company Publishers, pp. 127-154.
2. Yu, F. T. S. (1983). *Optical information processing*. Wiley Interscience Publication, John Wiley & Sons, pp. 123–135.
3. Yu, F. T. S. (1987). *Real time programmable optical correlator*, US Patent 4695973.
4. Sherman, R. C. (1987). *Optical correlator using electronic image preprocessing*, USA Patent 4637056.
5. Lee, Y.-P. T. (1985). *Multilayer neural network vision model for pattern recognition and stereo vision*. UCSD Ph.D. Dissertation, Chapter 5.

6. Pick, K., & Perets, Y. (2007). Method and apparatus of cross-correlation. USA Patent 7203253.
7. Sunwood, M. H., & Oh, S. K. (2004). Multiplierless 2-D convolver chip for real-time image processing. *Journal of VLSI Signal Processing, 38*, 63–71.
8. Zhang, M. Z, Ngo, H. T., & Asari, V. K. (2005). *Design of an efficient multiplier-less architecture for multi-dimensional convolution*, *advances in computer systems architecture* 10th Asia-Pacific Conference, ACSAC 2005, Singapore.
9. Zhang, M. Z., Ngoa, H. T., & Asari, V. K. (2007). Multiplier-less VLSI architecture for real-time computation of multi-dimensional convolution. *Microprocessors and Microsystems, 31*(1), 25–37.
10. Zhang, M. Z., & Asari, V. K. (2007). A design methodology for performance-resource optimization of a generalized 2D convolution architecture with quadrant symmetric kernels. *Advances in Computer Systems Architecture, 4697*, 220–234.
11. Wiatr, K., & Jamro, E., (2000). *Implementation image data convolutions operations in FPGA reconfigurable structures for real-time vision systems*. *Information Technology: Coding and Computing*, 2000. Proceedings. International Conference, pp. 152–157.
12. HSP48901 Data Sheet, Intersil, File Number 2459.5, (1999).
13. HSP48908 Data Sheet, Intersil, File Number 2456.5, (1999).
14. Decusatis, C., Koay, J., & Das, P. (1996). Hybrid optical implementation of discrete wavelet transforms: a tutorial. *Optics & Laser Technology, 28*(2), 51–58.
15. Chang, S., & Grover, C. P. (2004). Engineering implemtation of a hybrid optical correlator using SLMs. *Optics and Lasers in Engineering, 42*, 263–275.
16. Finisar,10- Gbps 850 nm VCSEL data sheet.
17. Alphalas, Ultrafast Photo detectors, UPD Series data sheet.
18. Saraswat, K. C., & Mohammadi, F. (1982). Effect of scaling of interconnections on the time delay of VLSI circuits. *IEEE Transactions on Electron Devices, ED-29*(4), 645–650.
19. Herbst, L. J. (1989). A critical look at Interconnect scaling. *IEE Colloquium on New Directions in VLSI Design*, 9/1-9/6.
20. Ferry, D. K., & Akers, L. A. (1997). Scaling theory in modern VLSI. *Circuits and Devics*, 41-44.
21. Krishnamoorthy, A. V., & Miller, D. A. B. (1996). Scaling optoelectronic VLSI circuits into the 21st century: a technology roadmap. *IEEE Journal of Selected Topics in Quantum Electronics, 2*(1), 55–76.

Dr. Lee received M.S.E.E. and M.S. Mathematics from University of Cincinnati 1978 and 1980 respectively and a Ph.D., Electrical and Computer Engineering from University of California, San Diego in 1995. His major research interests are optical computing, optoelectronic system design, VLSI or optoelectronic implementation of neural networks. His technical expertise is in artificial neural network, vision and pattern recognition, optoelectronics, VLSI architecture and image sensor system design. During his career, Dr. Lee has worked for SONY, Philips, NEC and SST. Dr Lee is currently an Assistant Professor of Department of Electronic Engineering, Ming Chuan University, Taoyuan, Taiwan, Republic of China.